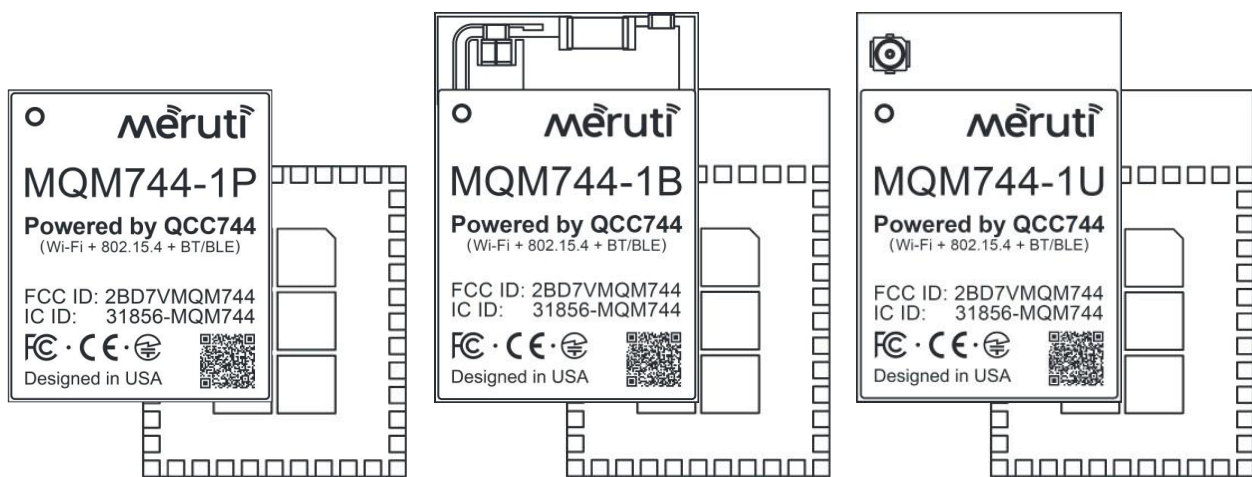




QCC744 Module Portfolio Data Sheet

March 2024



Documentation Title	Documentation No	Revision	Classification	Status	Date
QCC744 Module Portfolio Data Sheet		V2.0	Public	Release	Mar 31, 2024

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1 Product Overview

Powered by Qualcomm high performance 1x1 2.4GHz Wi-Fi 6/BT/15.4 combo all-in-one SoC QCC744, Qualcomm QCC744 IoT connectivity LGA module portfolio (MQM744-1) is purposely-designed to pack processing capabilities, Wi-Fi/BT/15.4 combo connectivity, and on-module memory into a single 44-pin LGA form factor with flexible choices of Pin, PCB and U.FL antenna. All variant antenna modules are pin compatible, allowing easy swap among modules. Its 1.27mm (0.05") pitch design enables seamless LGA pad into standard 1.27mm (0.05") header conversion to allow field replaceable header module portfolio if needed.

Unlike other Wi-Fi/BT/15.4 combo modules on the market, MQM744-1 has integrated powerful 32-bit RISC-V processor with FPU and DSP running up to 325MHz, on-chip 484KB SRAM and 128KB ROM, optional 4/8MB pSRAM and 8/16MB flash System-in-Package (SiP), multimedia features such as audio and video codec and interfaces, and 35x multiplexed GPIO rich peripherals. Its all-in-one design and capability contribute to reduced costs and enhanced performance, making it an attractive choice for IoT edge devices requiring single chip solution.

MQM744-1 operates in hostless mode, capable of running both the protocol stack all the way to application level as well as IoT applications without requiring an external MCU. Built on FreeRTOS, Its software SDK will be open-sourced on GitHub coupled with VS Code IDE market extension to facilitate rapid IoT application development. It can also be used as an IoT connectivity transceiver in hosted mode with an external host running all upper protocol stacks and applications.

MQM744-1 has undergone rigorous regulatory compliance testing and is certified with FCC, CE, IC, UKCA, RCM, MIC, KC, SRRC and environmentally compliant with RoHS and WEEE directives. It also completes protocol certification such as Wi-Fi Alliance, Bluetooth SIG 5.3 and OpenThread 1.3, Matter over Wi-Fi and Thread, AWS qualified device.

MQM744-1 includes the following configurations:

Module	Form Factor	Antenna
MQM744-1P	13.547 x 16.087 x 2.2 mm, 1.27 mm pitch, 44-pin, LGA	Pin Antenna
MQM744-1B	13.547 x 20.087 x 2.2 mm, 1.27 mm pitch, 44-pin, LGA	PCB Antenna
MQM744-1U	13.547 x 20.087 x 2.2 mm, 1.27 mm pitch, 44-pin, LGA	U.FL Antenna

MQM744-1 is graphically illustrated below:

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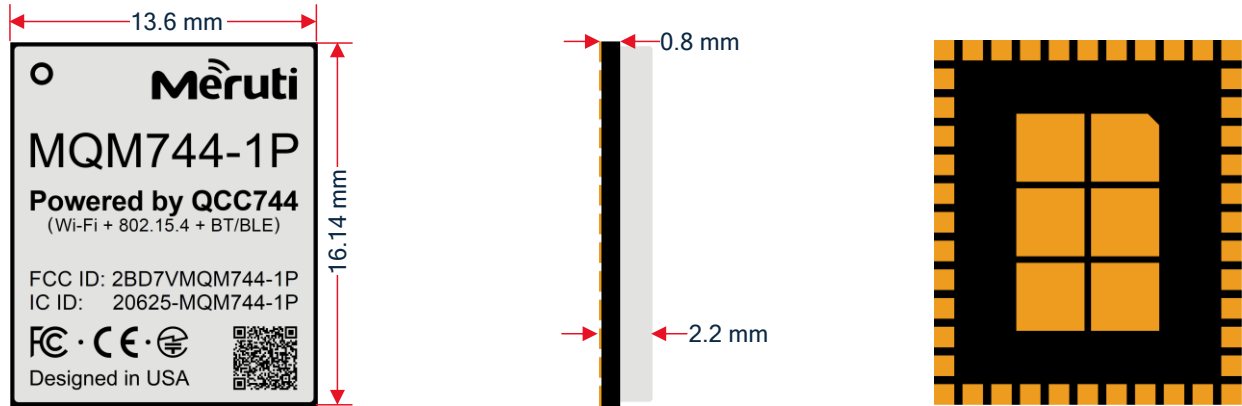


Figure 1: MQM744-1P Module View

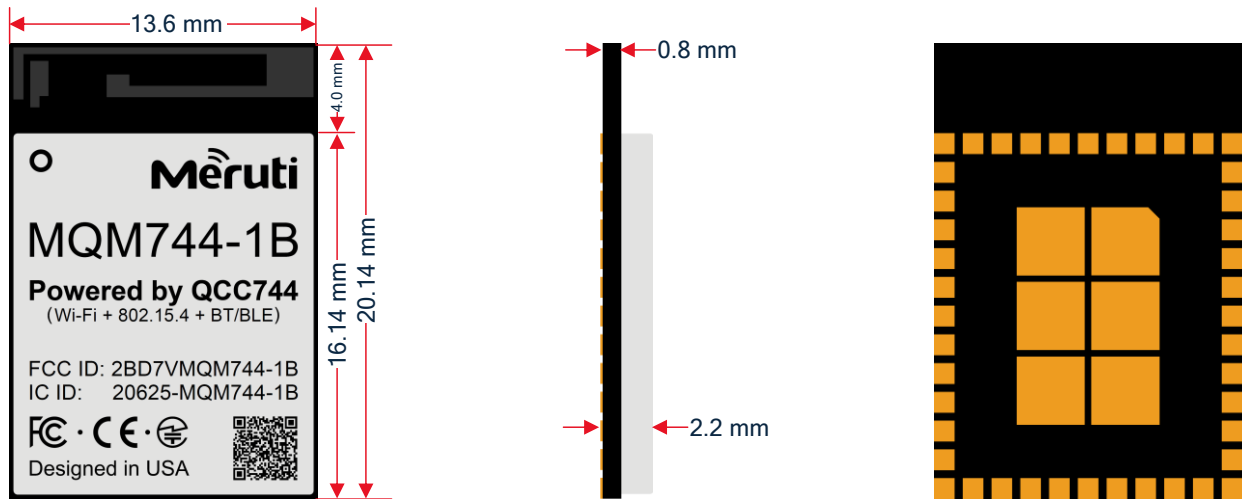


Figure 2: MQM744-1B Module View

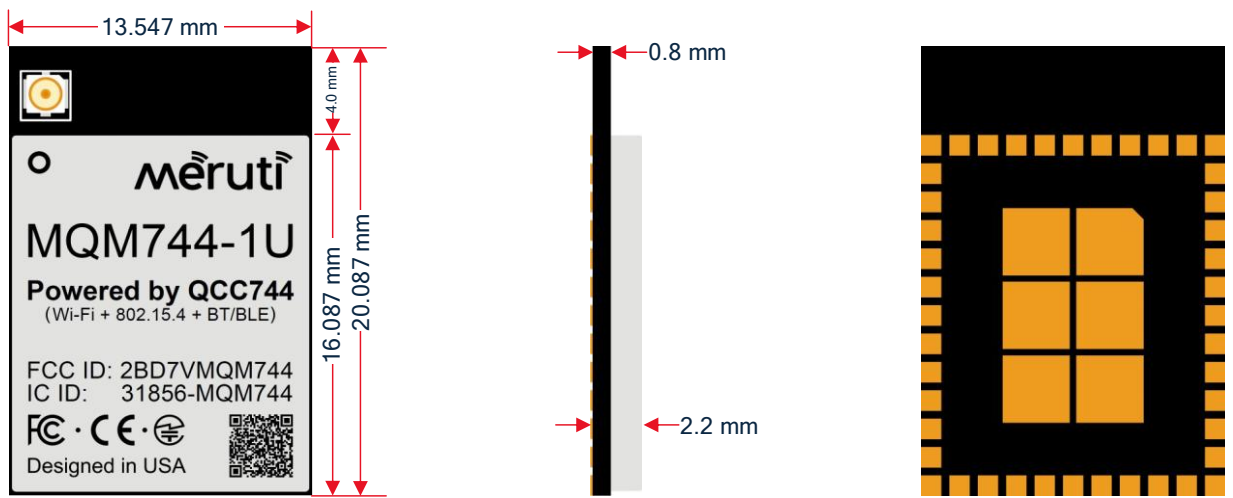


Figure 3: MQM744-1U Module View

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The MQM744-1 specific development kits are also provided to facilitate application software development as shown below:

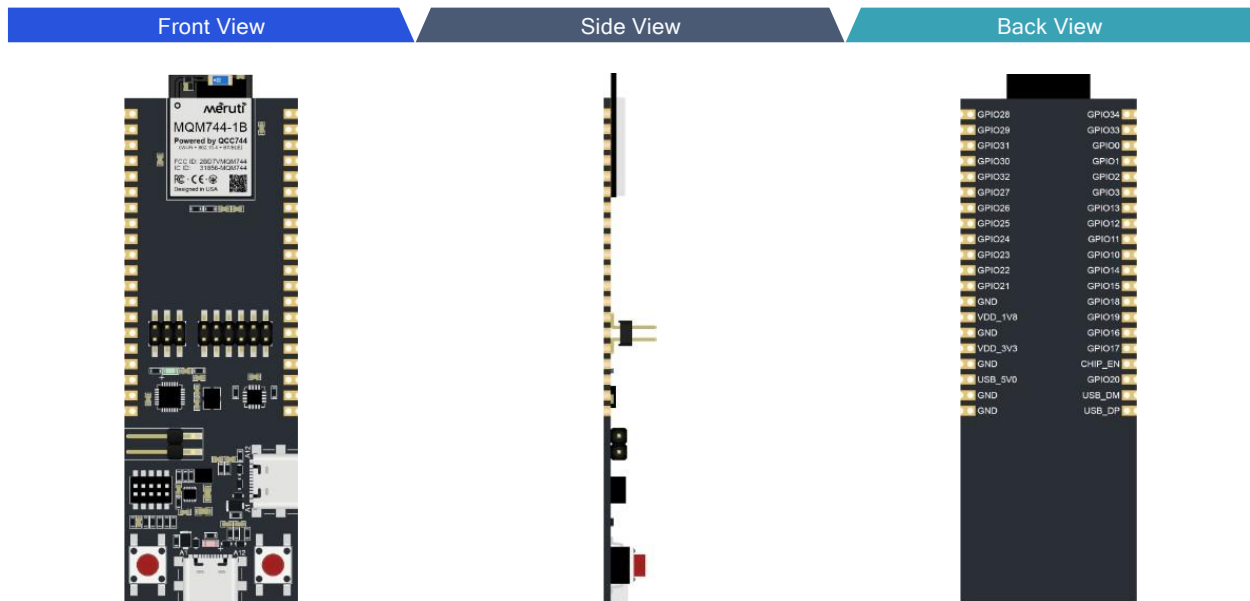


Figure 4: MQM744-1 Module Development Kit

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2 Hardware Specification

This section provides detailed hardware design and specification of MQM744-1. MQM744-1 hardware design has been optimized for small footprint and reduced RBOM cost.

2.1 Block Diagram

MQM744-1 integrates 4/8/16/32MB 3x4 WSON or 4x4 XSON NOR flash and optional 32.768kHz RTC crystal. The design also supports PCB antenna (MQM744-1B) or simply provides antenna pin (MQM744-1U) to allow customized antenna implementation on motherboard. The block diagram is shown below.

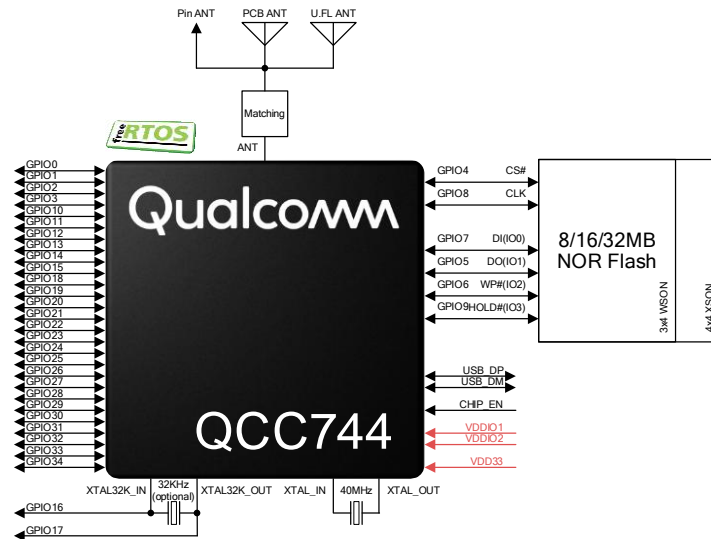


Figure 5: MQM744-1 Module Block Diagram

2.2 Pinout Description

2.2.1 Pin Map

In order to maintain pin compatible to allow easy drop replacement, All MQM744-1 shares the same pin map as illustrated below:

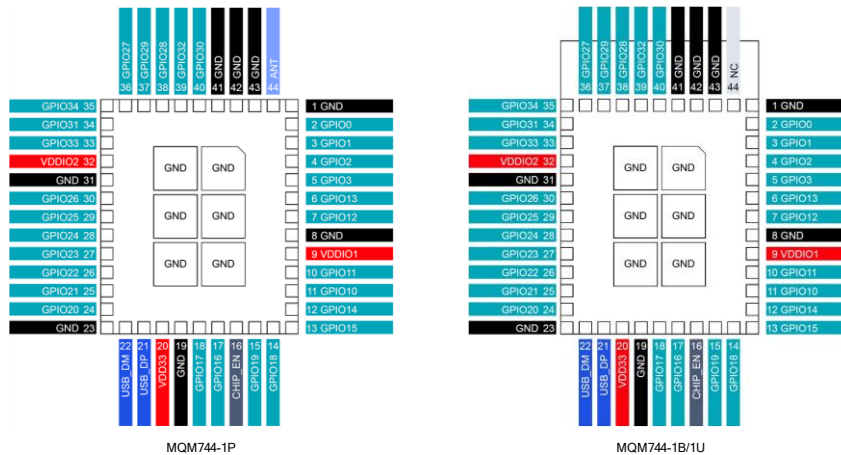


Figure 6: MQM744-1 Module Pin Map

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2.2.2 Pin Definition

Pin	Pin Name	Type	Power Domain	Description
20	VDD33	PWR	-	Power input (2.97~3.63V)
9	VDDIO1	PWR	-	Host I/O voltage input GPIO0~15
32	VDDIO2	PWR	-	Host I/O voltage input GPIO20~34
1,8,19,23,31	GND	GND	GND	Ground
44	ANT	AI/AO	-	Pin antenna
21	USB_DP	AI/AO	-	USB Data+
22	USB_DM	AI/AO	-	USB Data-
16	CHIP_EN	DI	-	Chip power on
2	GPIO0	DI/DO	VDDIO1	Generic PIO
3	GPIO1	DI/DO	VDDIO1	Generic PIO
4	GPIO2	DI/DO	VDDIO1	Generic PIO
5	GPIO3	DI/DO	VDDIO1	Generic PIO
11	GPIO10	DI/DO	VDDIO1	Generic PIO
10	GPIO11	DI/DO	VDDIO1	Generic PIO
7	GPIO12	DI/DO	VDDIO1	Generic PIO
6	GPIO13	DI/DO	VDDIO1	Generic PIO
12	GPIO14	DI/DO	VDDIO1	Generic PIO
13	GPIO15	DI/DO	VDDIO1	Generic PIO
17	GPIO16	DI/DO	VDD33	Generic PIO
18	GPIO17	DI/DO	VDD33	Generic PIO
14	GPIO18	DI/DO	VDD33	Generic PIO
15	GPIO19	DI/DO	VDD33	Generic PIO
24	GPIO20	DI/DO	VDDIO2	Generic PIO
25	GPIO21	DI/DO	VDDIO2	Generic PIO
26	GPIO22	DI/DO	VDDIO2	Generic PIO
27	GPIO23	DI/DO	VDDIO2	Generic PIO
28	GPIO24	DI/DO	VDDIO2	Generic PIO
29	GPIO25	DI/DO	VDDIO2	Generic PIO
30	GPIO26	DI/DO	VDDIO2	Generic PIO
36	GPIO27	DI/DO	VDDIO2	Generic PIO
38	GPIO28	DI/DO	VDDIO2	Generic PIO
37	GPIO29	DI/DO	VDDIO2	Generic PIO

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40	GPIO30	DI/DO	VDDIO2	Generic PIO
34	GPIO31	DI/DO	VDDIO2	Generic PIO
39	GPIO32	DI/DO	VDDIO2	Generic PIO
33	GPIO33	DI/DO	VDDIO2	Generic PIO
35	GPIO34	DI/DO	VDDIO2	Generic PIO

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2.2.3 I/O Pin Mux Table

GPIO	QSPI	SDIO	SDH	SPI	I2C (0/1)	UART (0/1)	I2S	PWM	CAN	ADC	DAC	EMAC	DVP	DBI	JTAG
GPIO0				CS	SCL	RTS/CTS/TX/RX	BCLK	CH0P/CH0P	TX/RX	CH9			CAM1_VSYNC		TMS
GPIO1				CLK	SDA	RTS/CTS/TX/RX	FS	CH1P/CH0N	TX/RX	CH8			CAM1_HSYNC		TCK
GPIO2				MISO	SCL	RTS/CTS/TX/RX	DI	CH2P/CH1P	TX/RX	CH2					TDO
GPIO3				MOSI	SDA	RTS/CTS/TX/RX	DO	CH3P/CH1N	TX/RX	CH3			CAM1_DAT0		TDI
GPIO10	SCL	DAT2	DAT1	MISO	SCL	RTS/CTS/TX/RX	DI	CH2P/CH1P	TX/RX	CH7			CAM1_DAT1	B_DB2/C_SDA0	TDO
GPIO11	CS	DAT3	DAT0	MOSI	SDA	RTS/CTS/TX/RX	DO	CH3P/CH1N	TX/RX				CAM1_DAT2	B_DB3/C_DCn	TDI
GPIO12	SDA0	CMD	CLK	CS	SCL	RTS/CTS/TX/RX	BCLK	CH0P/CH2P	TX/RX	CH6			CAM1_DAT3	B_DB4/C_SCL	TMS
GPIO13	SDA1	CLK	CMD	CLK	SDA	RTS/CTS/TX/RX	FS	CH1P/CH2N	TX/RX	CH5			CAM1_CLK	B_DB5/C_CSn	TCK
GPIO14	SDA2	DAT0	DAT3	MISO	SCL	RTS/CTS/TX/RX	DI	CH2P/CH3P	TX/RX	CH4	A_PWM_P		CAM1_DAT4	B_DB6/C_SDA0	TDO
GPIO15	SDA3	DAT1	DAT2	MOSI	SDA	RTS/CTS/TX/RX	DO	CH3P/CH3N	TX/RX		A_PWM_N		CAM1_DAT5	B_DB7/C_DCn	TDI
GPIO16				CS	SCL	RTS/CTS/TX/RX	BCLK	CH0P/CH0P	TX/RX				CAM1_DAT6		TMS
GPIO17				CLK	SDA	RTS/CTS/TX/RX	FS	CH1P/CH0N	TX/RX				CAM1_DAT7		TCK
GPIO18				MISO	SCL	RTS/CTS/TX/RX	DI	CH2P/CH1P	TX/RX						TDO
GPIO19				MOSI	SDA	RTS/CTS/TX/RX	DO	CH3P/CH1N	TX/RX	CH1					TDI
GPIO20				CS	SCL	RTS/CTS/TX/RX	BCLK	CH0P/CH2P	TX/RX	CH0/ACH0					TMS
GPIO21				CLK	SDA	RTS/CTS/TX/RX	FS	CH1P/CH2N	TX/RX	ACH1					TCK
GPIO22				MISO	SCL	RTS/CTS/TX/RX	DI	CH2P/CH3P	TX/RX	ACH2	A_PWM_P				TDO
GPIO23				MOSI	SDA	RTS/CTS/TX/RX	DO	CH3P/CH3N	TX/RX	ACH3	A_PWN_N				TDI
GPIO24				CS	SCL	RTS/CTS/TX/RX	BCLK	CH0P/CH0P	TX/RX				CAM0_DAT0		TMS
GPIO25				CLK	SDA	RTS/CTS/TX/RX	FS	CH1P/CH0N	TX/RX			REF_CLK	CAM0_DAT1		TCK
GPIO26				MISO	SCL	RTS/CTS/TX/RX	DI	CH2P/CH1P	TX/RX			TXD[0]	CAM0_DAT2		TDO
GPIO27				MOSI	SDA	RTS/CTS/TX/RX	DO	CH3P/CH1N	TX/RX	CH10/ACH4	A_PWN_N	TXD[1]	CAM0_DAT3		TDI
GPIO28				CS	SCL	RTS/CTS/TX/RX	BCLK	CH0P/CH2P	TX/RX	CH11/ACH5	A_PWM_P	RXD[0]	CAM0_HSYNC		TMS
GPIO29				CLK	SDA	RTS/CTS/TX/RX	FS	CH1P/CH2N	TX/RX	ACH6		RXD[1]	CAM0_VSYNC		TCK
GPIO30				MISO	SCL	RTS/CTS/TX/RX	DI	CH2P/CH3P	TX/RX	ACH7		RXERR	CAM0_CLK		TDO
GPIO31				MOSI	SDA	RTS/CTS/TX/RX	DO	CH3P/CH3N	TX/RX			TX_EN	CAM0_DAT4		TDI
GPIO32				CS	SCL	RTS/CTS/TX/RX	BCLK	CH0P/CH0P	TX/RX			RX_DV	CAM0_DAT5		TMS
GPIO33				CLK	SDA	RTS/CTS/TX/RX	FS	CH1P/CH0N	TX/RX			MDC	CAM0_DAT6		TCK
GPIO34				MISO	SCL	RTS/CTS/TX/RX	DI	CH2P/CH1P	TX/RX			MDIO	CAM0_DAT7		TDO

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2.3 Computing Subsystem

MQM744-1 has Qualcomm QCC744 at his core which integrates 32-bit RISC-V @325MHz, 128KB ROM and 484KB SRAM as well as on-module NOR flash with size up to 32MB. The code can be executed from flash via Execution-in-Place (XiP).

Qualcomm QCC744 does allow to pack additional memory such as pSRAM and NOR flash in the same 7x7 QFN-56 package to support applications where more memory and smaller size are required. MQM744-1 support all those SKUs.

Qualcomm QCC744	pSRAM Built-in	Flash Built-in	Grade	Package
QCC744-1	X	X	-40~105°C	QFN-56, 7 x 7 x 0.9 mm, 0.4 mm pitch
QCC744-2	4MB	X	-40~85°C	QFN-56, 7 x 7 x 0.9 mm, 0.4 mm pitch
QCC744-3	8MB	X	-40~85°C	QFN-56, 7 x 7 x 0.9 mm, 0.4 mm pitch
QCC744-4	4MB	8MB	-40~85°C	QFN-56, 7 x 7 x 0.9 mm, 0.4 mm pitch
QCC744-5	16MB	X	-40~85°C	QFN-56, 7 x 7 x 0.9 mm, 0.4 mm pitch

The computing subsystem software architecture is shown below:

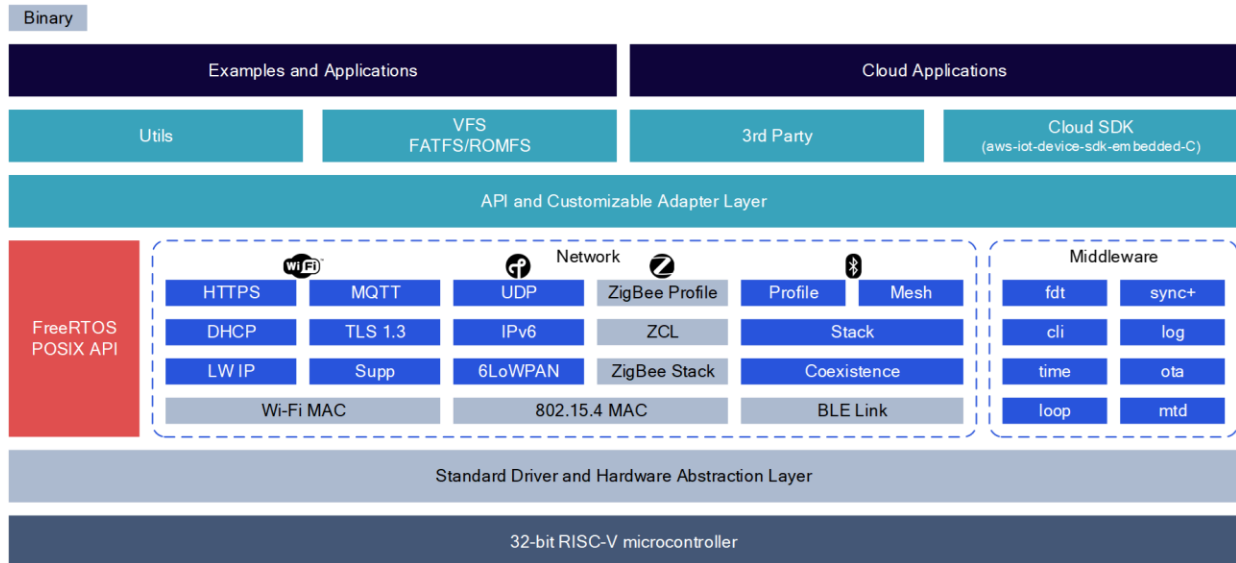


Figure 7: Computing Subsystem Software Architecture

Software SDK will be open sourced at Codelinaro with blocks in dot line will be offered in binary format inside software SDK package.

Codelinaro Download Link: <https://git.codelinaro.org/clo/qcc7xx/QCCSDK-QCC74x>

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3 Electrical Characteristics

3.1 Absolute Maximum Ratings

The absolute maximum ratings provided in this section reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating.

Pin	Parameter	Min	Max	Unit
VDD33	Power input voltage	-0.3	3.63	V
VDDIO1, VDDIO 2	I/O port voltage	-0.3	3.63	V
ESD Protection (HBM)			2,000	V
Storage temperature		-40	135	°C

3.2 Recommended Operating Conditions

Pin	Parameter	Min	TYP	Max	Unit
VDD33	Power input voltage	2.97	3.3	3.63	V
VDDIO1, VDDIO 2 (3.3V)	I/O port voltage	2.97	3.3	3.63	V
VDDIO1, VDDIO 2 (1.8V)	I/O port voltage	1.62	1.8	1.98	V

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4 Radio Performance

The radio performance for Wi-Fi, Bluetooth and 802.15.4 are shown in the table below:

4.1 802.11b/g/n/ax (Wi-Fi 6)

Standard	PHY	Modulation	MCS Index	Data Rate (Mbps)		Max Tx Power (dBm)		Rx Sensitivity (dBm)	
				HT20	HT40	HT20	HT40	HT20	HT40
802.11b	CCK (DSSS)	DBPSK	-	1	-	22	-	-	-
	CCK (DSSS)	DQPSK	-	2	-	-	-	-	-
	CCK (DSSS)	B/DQPSK	-	5.5	-	-	-	-	-
	CCK (DSSS)	Q/DQPSK	-	11	-	22	-	-	-
802.11g	OFDM	BPSK	-	6	-	21	-	-	-
	OFDM	BPSK	-	9	-	-	-	-	-
	OFDM	QPSK	-	12	-	-	-	-	-
	OFDM	QPSK	-	18	-	-	-	-	-
	OFDM	16QAM	-	24	-	-	-	-	-
	OFDM	16QAM	-	36	-	-	-	-	-
	OFDM	64QAM	-	48	-	-	-	-	-
	OFDM	64QAM	-	54	-	19	-	-	-
802.11n	OFDM	BPSK	MCS0	7.2	15	20	20	-93	-89.5
	OFDM	QPSK	MCS1	14.4	30	-	-	-91	-88
	OFDM	QPSK	MCS2	21.7	45	-	-	-89	-86
	OFDM	16QAM	MCS3	28.9	60	-	-	-86.5	-83.5
	OFDM	16QAM	MCS4	43.3	90	-	-	-83	-80.5
	OFDM	64QAM	MCS5	57.8	120	-	-	-79	-76.5
	OFDM	64QAM	MCS6	65	135	-	-	-77.5	-75
	OFDM	64QAM	MCS7	72.2	150	19	18	-76	-73
802.11ax	OFDMA	BPSK	MCS0	8.6	17.2	20	20	-93	-89.5
	OFDMA	QPSK	MCS1	17.2	34.4	-	-	-91	-88
	OFDMA	QPSK	MCS2	25.8	51.6	-	-	-89	-86.5
	OFDMA	16QAM	MCS3	34.4	68.8	-	-	-86	-83.5
	OFDMA	16QAM	MCS4	51.6	103.2	-	-	-83	-80
	OFDMA	64QAM	MCS5	68.8	137.6	-	-	-79	-76.5
	OFDMA	64QAM	MCS6	77.4	154.9	-	-	-77.5	-75
	OFDMA	64QAM	MCS7	86	172.1	-	-	-75.5	-73
	OFDMA	256QAM	MCS8	103.2	206.5	-	-	-72	-69
	OFDMA	256QAM	MCS9	114.7	229.4	18	16	-70	-67

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4.2 Bluetooth

Standard	Topology	PHY	Modulation	Data Rate	Max Tx Power (dBm)	Rx Sensitivity (dBm)
BT Classic	P2P	BR	GFSK	1Mbps	+10	-94
		EDR	$\pi/4$ DQPSK	2Mbps	+8	-96
		EDR	8DPSK	3Mbps	+8	-90
BLE	P2P Broadcast Mesh	LE 2M	GFSK	2Mbps	+10	-97
		LE 1M	GFSK	1Mbps	+10	-99
		LE Coded (S=2)	GFSK	500Kbps	+10	-102
		LE Coded (S=8)	GFSK	125Kbps	+10	-105

4.3 802.15.4

TBD

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5 Power Consumption

MQM744-1 can operate in four power states as shown below to maximize power saving:

- Active – Continuous transmitting or receiving on connection to AP
- Idle – No active transmitting or receiving. CPU is in idle state.
- Deep Sleep – Wi-Fi/USB/CPU/Peripherals power off. This is DTIM power saving mode
- Hibernation – No connection to AP.
- Shut down – the chip is completed shut down

The power consumption for each state is listed in the table below:

Operation Mode	State	Typical	Unit	Comments
Active	MCU Active & Rx Active	38	mA	MCU 160MHz, XCLK 40MHz, BCLK 80MHz, Flash 40MHz
	Tx Active	266	mA	MCS0, Tx Power = +18 dBm
Power Saving	Deep Sleep	64	µA	Wi-Fi/USB/CPU/Peripherals Power Off. This is DTIM PS mode
	Hibernation	2.1	µA	4KB RAM retained
	Shut Down	0.15	µA	
DTIM	DTIM 1	476	µA	Xtal32k
		524	µA	RC 32k
	DTIM 3	179	µA	Xtal32k
		227	µA	RC 32k
	DTIM 5	119	µA	Xtal32k
		167	µA	RC 32k
	DTIM 10	75	µA	Xtal32k
		123	µA	RC 32k

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6 Mechanical Specification

6.1 Pin Antenna

6.1.1 Dimension

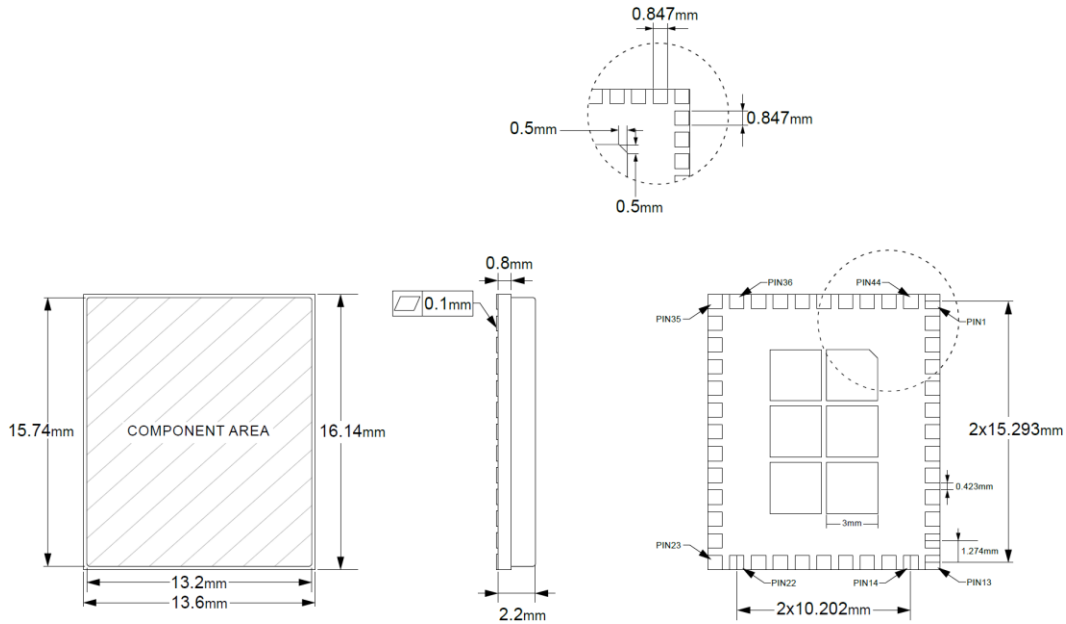


Figure 8: MQM744-1P Module Dimension

6.1.2 Recommended PCB Landing Pattern

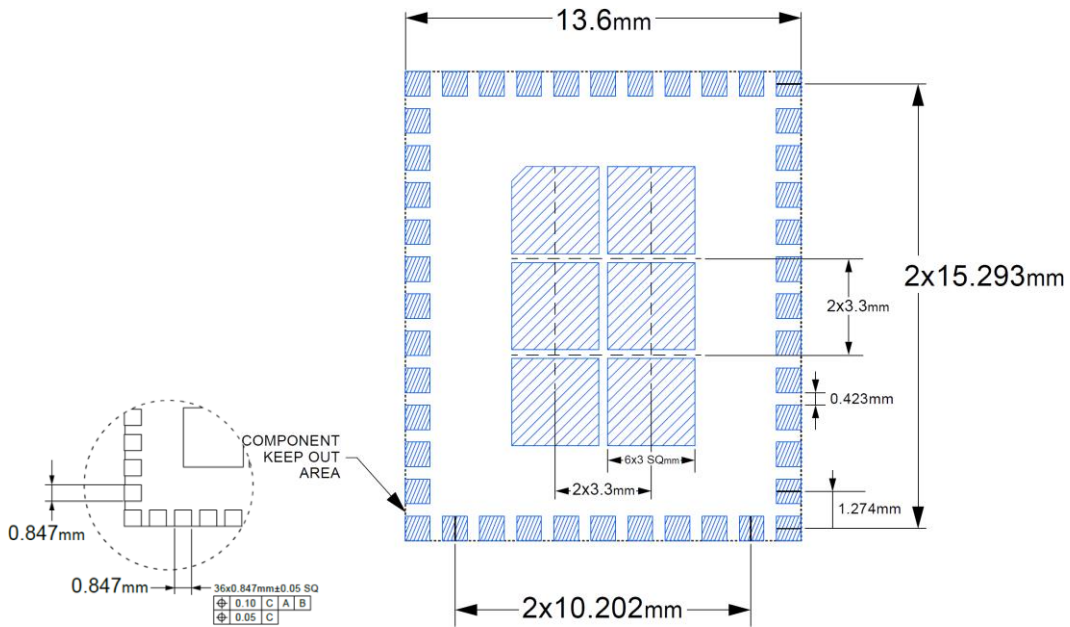


Figure 9: MQM744-1P Module PCB Landing Pattern

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6.2 PCB Antenna

6.2.1 Dimension

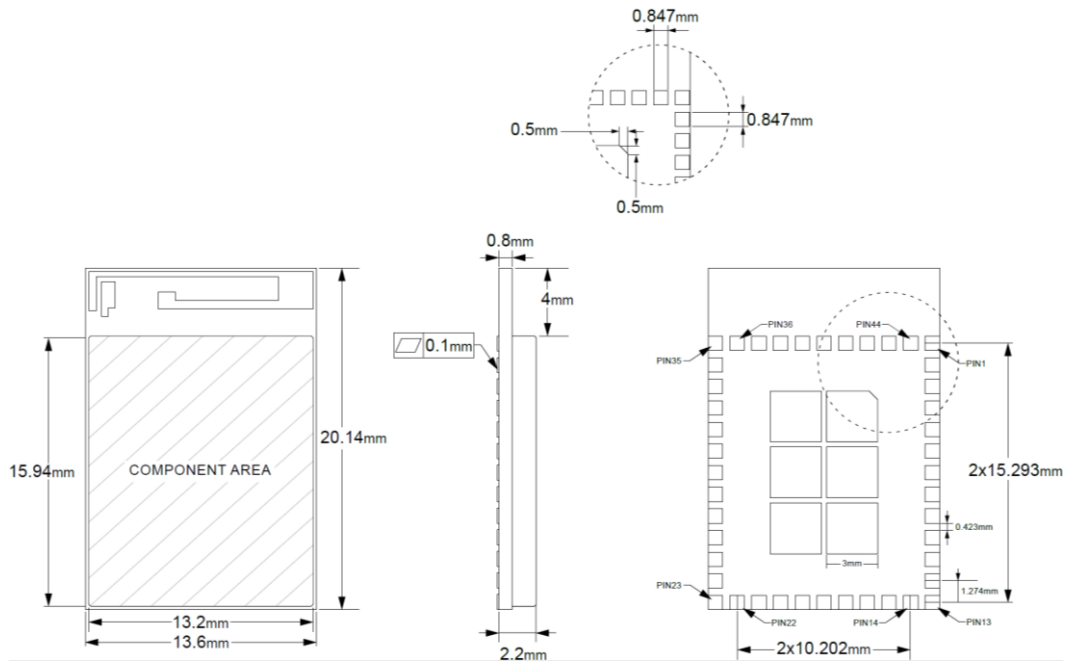


Figure 10: MQM744-1B Module Dimension

6.2.2 Recommended PCB Landing Pattern

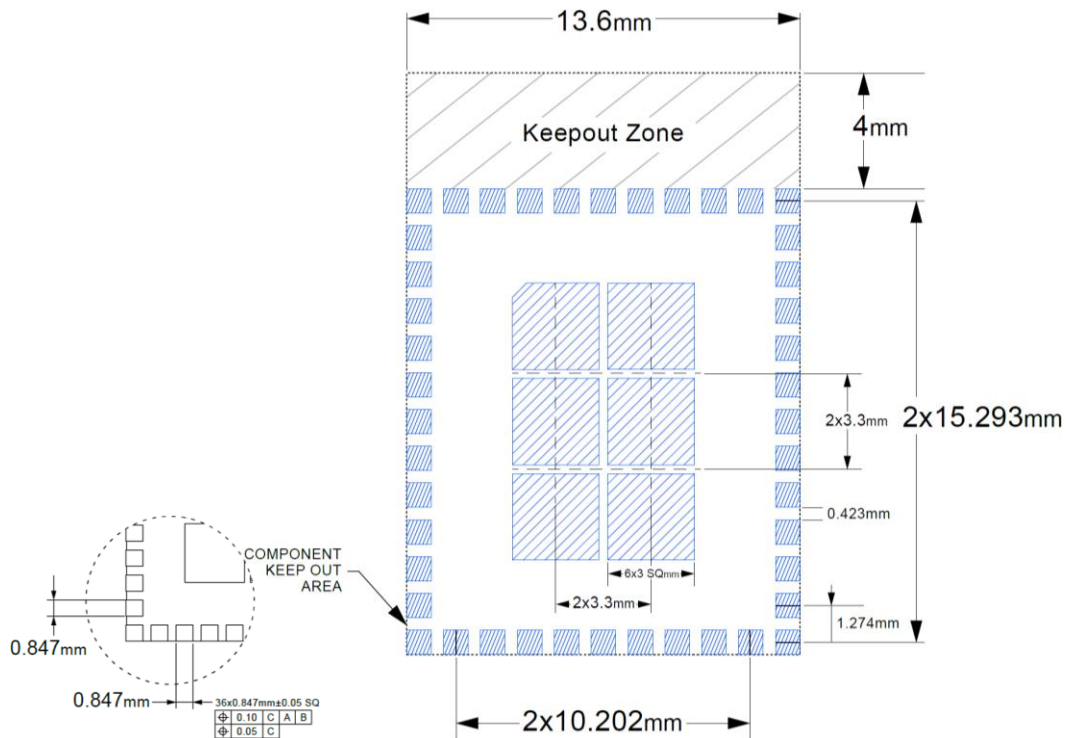


Figure 11: MQM744-1B Module PCB Landing Pattern

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6.3 U.FL Antenna

6.3.1 Dimension

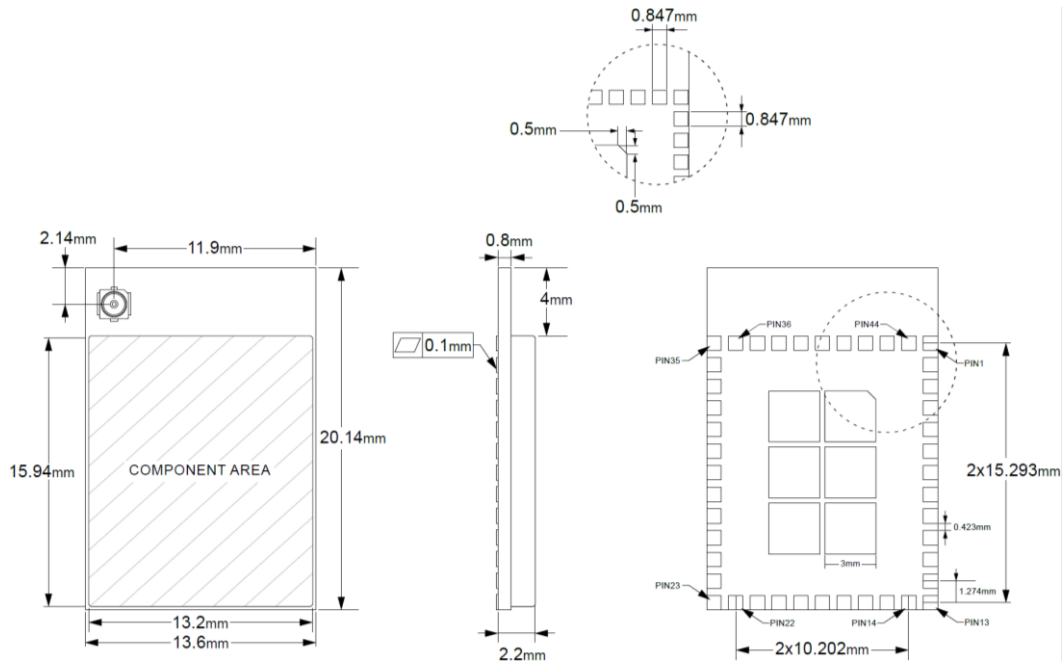


Figure 12: MQM744-1U Module Dimension

6.3.2 Recommended PCB Landing Pattern

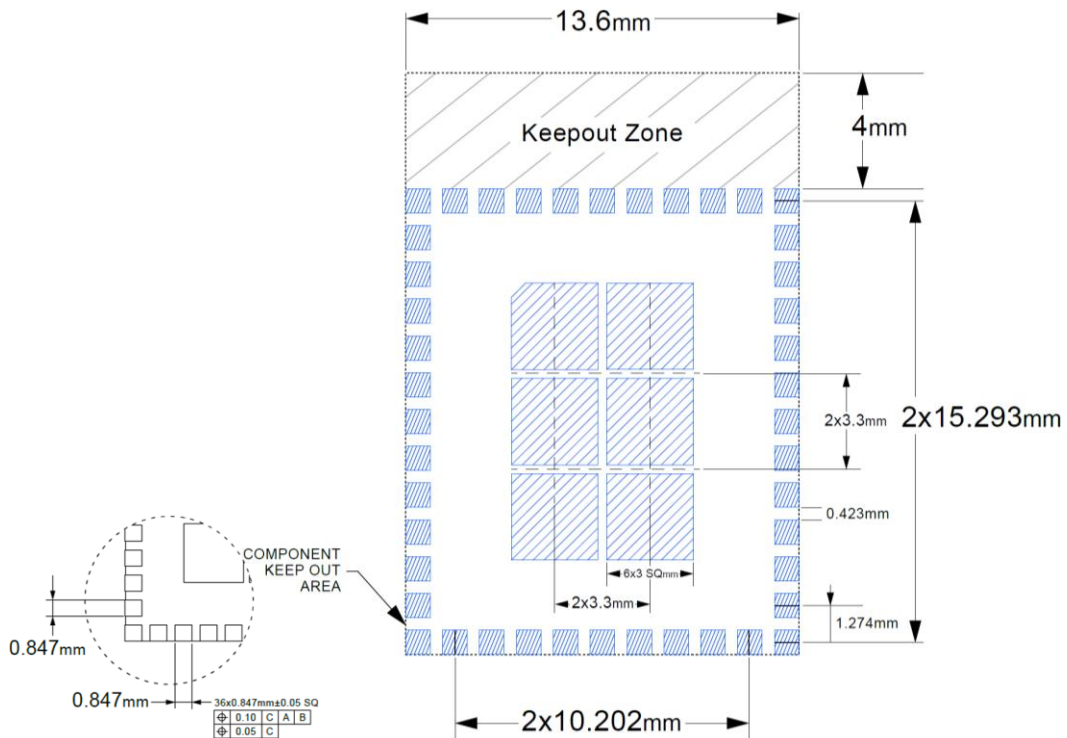


Figure 13: MQM744-1U Module PCB Landing Pattern

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7 Manufacturing Recommendation

7.1 Power Layout Guideline

MQM744-1 is powered by either 3V battery or DC 3.3V. Power pin connection capacitor is as close as possible to chip and pin. Decoupling the power supply from the chip using a capacitor. Use capacitors to prevent noise from coupling back to the power plane.

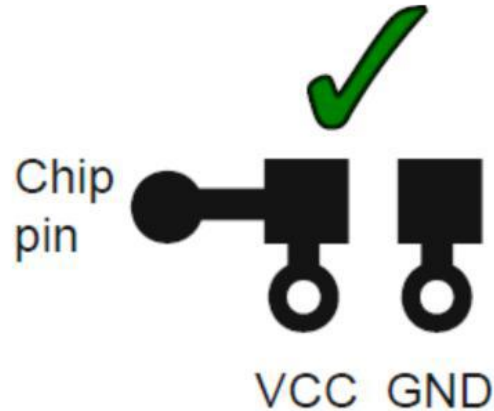


Figure 14: Power Layout Guideline

7.2 RF Layout Guideline

To optimize antenna performance, place MQM744-1 in the corner of the PCB as shown below. Do not cover copper and trace the antenna clearance area. Keep the antenna area as far away as possible from the power supply and metal components. Connect all GND pins directly to a solid GND plane. Place GND vias as close as possible to the GND pin. Use a good layout method to avoid excessive noise coupling with signal lines or supply voltage lines.

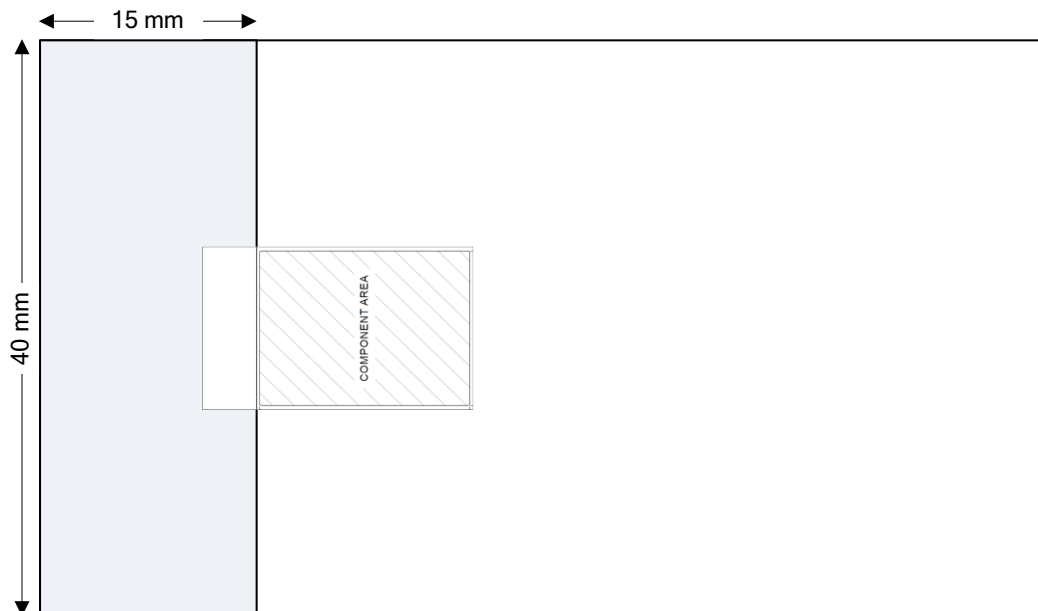


Figure 15: RF Layout Guideline

Documentation Title	Documentation No	Revision	Classification	Status	Date
QCC744 Module Portfolio Data Sheet		V2.0	Public	Release	Mar 31, 2024

7.3 Soldering Recommendations

MQM744-1 can be SMT on the board following the temperature curve graph:

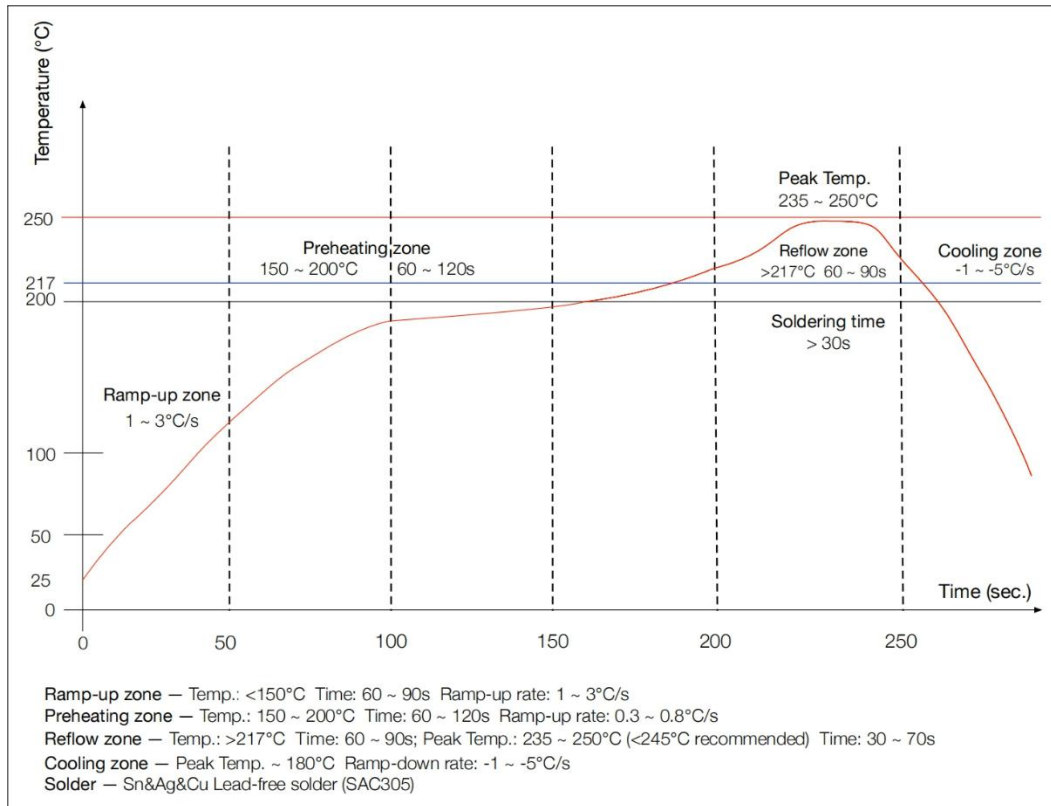


Figure 16: Soldering Guideline

Documentation Title	Documentation No	Revision	Classification	Status	Date
QCC744 Module Portfolio Data Sheet		V2.0	Public	Release	Mar 31, 2024

8 Packaging

MQM744-1 is packaged on reels loaded with 1000 modules. Each reel is placed in an antistatic bag with a desiccant pack and a humidity card and placed in an 36x25x12cm box. Anti-static warnings and labels adhere to the outside of the bag.

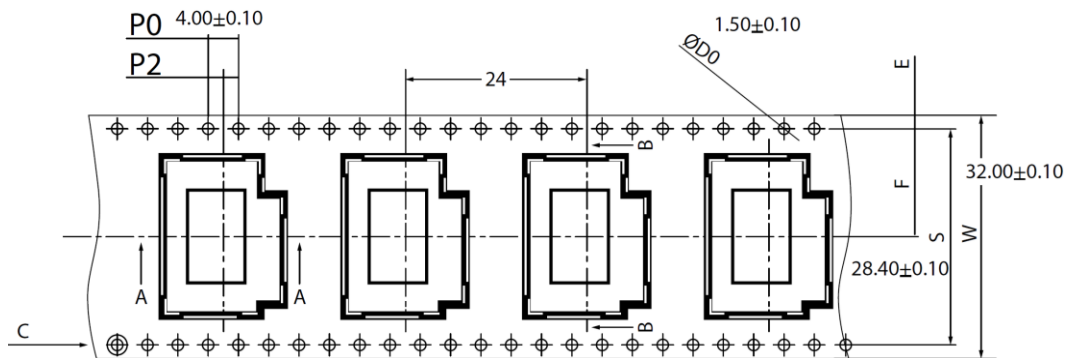


Figure 17: Module Packaging

Warning

The MeshConnect Modules contain highly sensitive electronic circuitry. Handling without proper ESD protection may destroy or damage the module permanently.

Warning

The MeshConnect Modules are moisture-sensitive devices. Appropriate handling instructions and precautions are summarized in J-STD-033. Read carefully to prevent permanent damage due to moisture intake.

Moisture Sensitivity Level (MSL)

MQM744-1 is qualified to moisture sensitivity (MSL3) in accordance with JEDEC J-STD-020

Storage

Storage/shelf life in sealed bags is 12 months at <40°C and <90% relative humidity. 12.2 Packing Label

Documentation Title	Documentation No	Revision	Classification	Status	Date
QCC744 Module Portfolio Data Sheet		V2.0	Public	Release	Mar 31, 2024

9 Regulatory Compliance

Country	Certification	No
USA	FCC 15C	2ACCRMQM744
Europe Union	CE	20625-MQM744
Canada	IC	20625-MQM744
Japan	MIC	Coming soon
Korea	KC	Coming soon
Australia	RCM	Coming soon
United Kingdom	UKCA	Coming soon
China	SRRC	Coming soon

Documentation Title	Documentation No	Revision	Classification	Status	Date
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10 Order Information

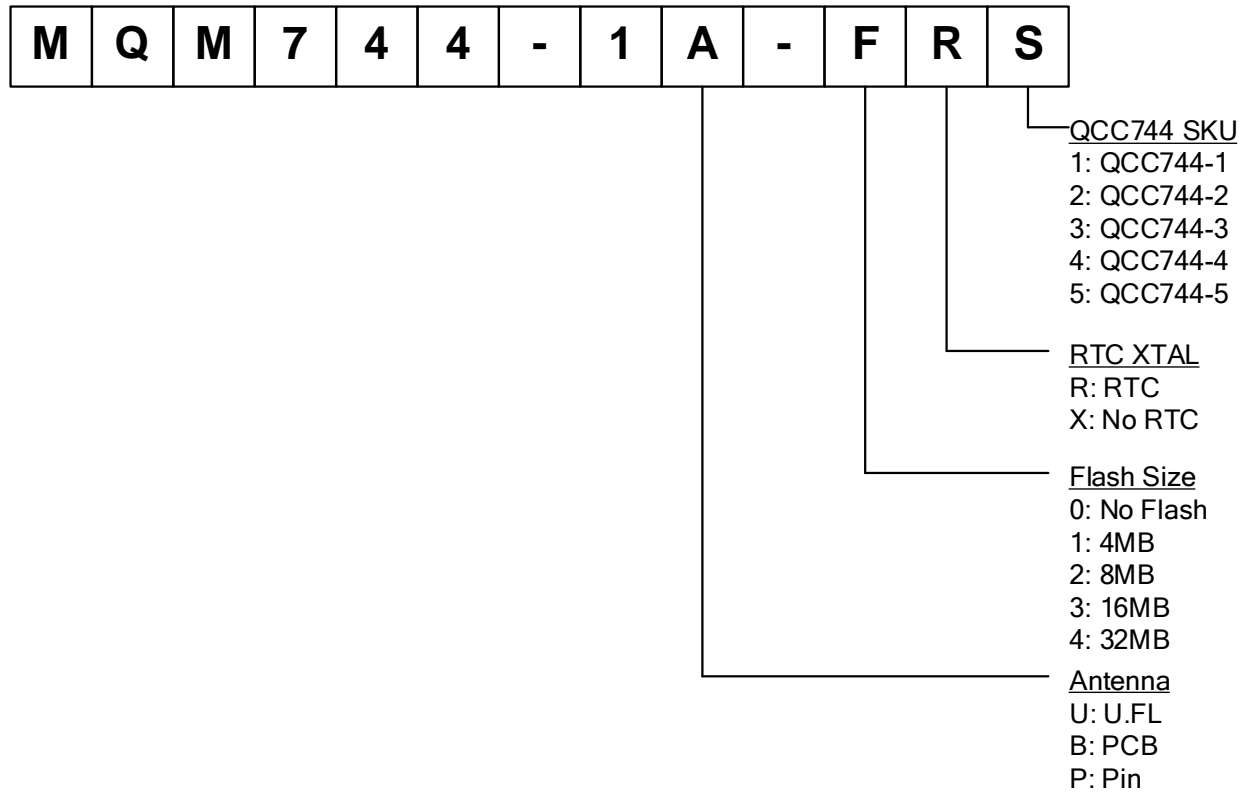


Figure 18: Order Number

Documentation Title	Documentation No	Revision	Classification	Status	Date
QCC744 Module Portfolio Data Sheet		V2.0	Public	Release	Mar 31, 2024

Revision History

Revision	Description	Date
0.1	Initial draft	January 5, 2024
0.2	Miscellaneous error correction	January 15, 2024
0.3	Changed module model name to MQM744-1	January 20, 2024
2.0	Re-designed to optimize RF performance	March 31, 2024

Documentation Title	Documentation No	Revision	Classification	Status	Date
QCC744 Module Portfolio Data Sheet		V2.0	Public	Release	Mar 31, 2024

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